Amendments to the Drawings

The attached sheet of drawing includes changes to Fig. 4. In Fig. 4, a duplicative reference text "Reset" has been replaced with a reference text of "Row Pulse."

Attachment: Replacement Sheet

Annotated Sheet Showing Changes

REMARKS

Claims 1 to 20 were pending in the above-identified application. This Amendment amends claims 1, 2, 4 to 6, 14 to 18, and 20, cancels claims 7 to 13, and adds claim 21.

Amendments to the Drawings

Applicant has amended Fig. 4 to replace a duplicative reference text of "Reset" with a reference text of "Row Pulse." Support for this amendment can be readily found in p. 13, line 22 to p. 14, line 2.

Specification

The Examiner noted a discrepancy between the Specification and a limitation in claim 6. Applicant has amended claim 6 as suggested by the Examiner to remove this discrepancy.

§102 Rejections

The Examiner rejected claims 1 to 3 and 5 to 14 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,424,375 ("Fowler"). Applicant has amended claim 1, which now recites:

> Claim 1: An image capture system, comprising:
>
> a plurality of rows of pixels, each row comprising:
>
> a reset line for providing a reset signal;
>
> a plurality of pixels, each pixel comprising:
>
> a first FET having a gate terminal coupled to the reset line, a drain terminal coupled to a supply voltage, and a source terminal coupled to a readout node; and
>
> a photodetector coupled between a first ground and the readout node;
>
> a switching device selectively coupled to one of the reset lines in the rows of pixels; and

> a reference voltage source coupled between a second ground and one of the reset lines via the switching device, wherein the reference voltage source generates a reset voltage that is independent of the supply voltage and the first and second grounds have the same potential.

Amended claim 1 (emphasis added). Amended claim 1 now recites a switching device that couples a reference voltage source to one of multiple reset lines in corresponding rows of pixels. This arrangement allows the reference voltage source to supply a reset voltage that is independent of the supply voltage to multiple pixels in a single row.

On the other hand, Fowler discloses a design where a reference voltage source is provided for each pixel. This is because the reference voltage source in Fowler consists of an operational amplifier 106 with an inverted input coupled to a readout node 110 and a switch 120 to provide a closed-loop feedback path for each pixel. Fowler, col. 4, lines 13 to 15, and Fig. 1. Thus, Fowler does not disclose a reference voltage source that supplies a reset voltage to multiple pixels in a single row. Furthermore, Fowler probably cannot be modified with additional pixels to receive the reference voltage from the same reference voltage source because that may alter the feedback loop design of Fowler. Accordingly, Applicant submits that amended claim 1 is patentable over Fowler.

Applicant further notes that the present invention seeks to address row-wise noise stemming from an arrangement where multiple pixels in a common row are tied to the same reset line. However, Fowler probably does not have such a row-wise noise since each pixel has its own reference voltage source. Thus, there is no motivation to combine Fowler with other references to obviate the present invention.

Claims 2, 3, 5, and 6 depend from claim 1 and are patentable over Fowler for at least the same reasons as claim 1.

Furthermore, claims 2 and 6 recite "an operational amplifier buffer comprising ... an inverting input coupled to the output in a feedback loop, wherein the feedback loop does not pass through the readout node." Amended claims 2 and 6. As described above, Fowler discloses an operational amplifier 106 with a feedback loop connected to its readout node 110. Thus, claims 2 and 6 are further patentable over Fowler.

Applicant has canceled claims 7 to 13, thereby rendering their rejections moot.

Applicant has amended claim 14 to depend from claim 1. Thus, claim 14 is patentable over Fowler for at least the same reasons as claim 1.

The Examiner rejected claims 15 to 20 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,133,862 ("Dhuse et al."). Applicant has amended claim 15 to recite "providing a first reset signal to a row of pixels, the first reset signal being derived from a reference voltage that is independent of a supply voltage." Dhuse et al. does not disclose a reset signal that is independent of a supply voltage. Accordingly, claim 15 is patentable over Dhuse et al.

Claims 16 to 20 depend from claim 15 and are therefore patentable over Dhuse et al. for at least the same reasons as claim 15.

The Examiner rejected claims 1 and 4 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,147,846 ("Borg"). Applicant has amended claim 1, which now recites a "reference voltage source [that] generates a reset voltage that is independent of the supply voltage." Amended claim 1. On the other hand, Borg discloses a reset voltage that is dependent on a supply rail V_{DD}. Fig. 2 of Borg shows that a reset signal line 180 is connected by a driver circuit 150 to a node 170 in an over-voltage generation component 149. This sets the reset voltage (Row Reset) equal to the voltage at node 170. The voltage at node 170 in turn is derived from supply rail V_{DD}.

> As a reset operation begins, the voltage level at node 170 is settled at approximately 0.7V (one diode drop) below V_{DD}, DRV switch 175 is open, and the INT switch is closed, holding the row reset line low. The INT switch 185 is then opened while the DRV switch 175 is simultaneously closed. This causes the voltage on the row reset line to rise to an equalized voltage level determined by charge transfer from drive capacitor 160 to the parasitic capacitance 188. The intermediate row reset voltage level equals approximately $C_D * (V_{DD} - 0.7)/(C_{RST} + C_D)$.
>
> The RSTB is then asserted (driven low) which raises the output of the inverter towards V_{DD}, which further drives the row reset signal to a level:
>
> $$\text{Row Reset} = C_D * (2 * V_{DD} - 0.7)/(C_{RST} + C_D) \qquad \text{Eqn. 1}$$

Borg, col. 3, lines 46 to 65 (emphasis added). As the equations for the reset voltage Row Reset show, it depends on supply rail V_{DD}. Thus, Borg does not disclose a "reference voltage source [that] generates a reset voltage that is independent of the supply voltage."

New claim

New claim 21 depends from claim 1 and is patentable over the cited references for at least the same reasons as claim 1.

In summary, claims 1 to 20 were pending in the above-identified application. Applicant has amended claims 1, 2, 4 to 6, 14 to 18, and 20, canceled claims 7 to 13, and added claim 21. For the above reasons, Applicant respectfully requests allowance of claims 1, 2, 4 to 6, 14 to 18, 20, and 21. Should the Examiner have any questions, please call the undersigned at (408) 382-0480x206.

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Respectfully submitted,

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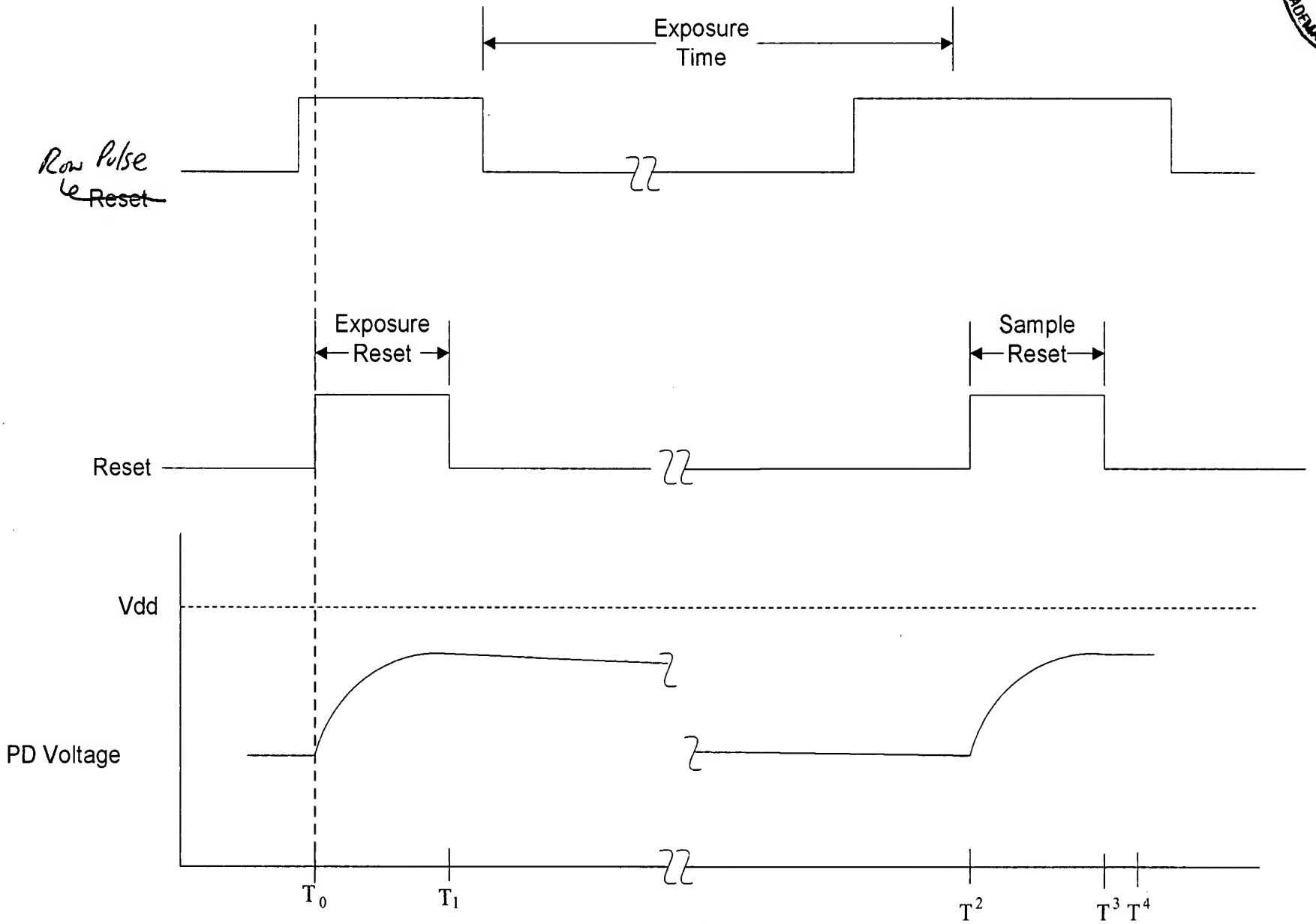

FIG. 4